ABSTRACT OF THE DISCLOSURE

A system and method for synchronizing data transfer operations between two circuit portions across a clock domain boundary. A primary clock signal is operable to clock a first circuit portion and a secondary clock signal, generated from the primary clock signal, is operable to clock a second circuit portion. A SYNC pulse signal is generated based on coincident rising edges of the primary and secondary clock signals. A clock synchronizer controller is operable to generate a plurality of control signals based on the SYNC pulse signal for actuating data transfer circuitry disposed between the first and second circuit portions. A SYNC adjuster portion included in the clock synchronizer controller is operable to re-position the SYNC pulse signal by redefining a new coincident rising edge with respect to the primary and secondary clock signals based on a clock skew relative to each other.